REMARKS

Applicants have studied the Office Action dated August 4, 2005, and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, Claims 1, 9-11, 18, 25, and 33-34, are amended, and Claims 8 and 32 have been cancelled. After this amendment, Claims 1-34 are pending. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks is respectfully requested.

In the Office Action, the Examiner:

(2) objected to the specification informalities;

(3) objected to claims 1-34 for not having a preamble that properly states the intended use or purpose of the invention;

(4-27) rejected claims 1-8, 10-32, and 34 under 35 U.S.C. § 102(b) as being anticipated by Balaji, E. et al. "Modeling ASIC Memories in VHDL." Proc. Of EURO-DAC '96. Sept. 16-20 1996, pp. 502-508 ("Balaji"); and

(28-30) indicated that claims 9 and 33 would be allowable if rewritten in independent form including all of the limitations of the base claim and all intervening claims.

(2) Objection to the Specification:

In the specification, the paragraph beginning on page 1, line 13 has been amended to add the missing patent application numbers. Accordingly, Applicants request that the Examiner withdraw the objection to the specification.

(3) Rejection under 35 U.S.C. §102(b)

As noted above, the Examiner rejected claims 1-8, 10-32, and 34 under 35 U.S.C. § 102(b) as being anticipated by Balaji, E. et al. "Modeling ASIC Memories in VHDL." Proc. Of EURO-DAC '96. Sept. 16-20 1996, pp. 502-508 ("Balaji").

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Amended independent claims 1 and 25 recite, *inter alia*:

> selecting a rise time delay value and a fall time delay value in a VHDL standard delay file **that correspond to an instance of a logic gate** in a logic model;
>
> storing in a rise time generic variable the selected rise time delay value;
>
> storing in a fall time generic variable the selected fall time delay value;
>
> building a rise-time super generic value for the selected rise time delay value; and
>
> building a fall-time super generic value for the selected fall time delay value,
>
> wherein the rise-time super generic value **represents rise times** and includes the rise time delay value stored in the rise time generic variable and the fall-time super generic value **represents fall times** and includes the fall time delay value stored in the fall time generic variable, **the rise-time super generic value being independent from the fall-time super generic value. (Emphasis added)**

Independent claim 11 recites, *inter alia*:

> a program memory storing an SDF reducer;
>
> a data memory for storing a VHDL standard delay file, for storing in a rise time generic variable the selected rise time delay value, and for storing in a fall time generic variable the selected fall time delay value;
>
> a controller/processor coupled to the program memory, the controller/processor for selecting a rise time delay value and a fall time delay value in a VHDL standard delay file that **correspond to an instance of a logic gate** in a logic model, for building a rise-time super generic value **for the selected rise time delay value**, and for building a fall-time super generic value **for the selected fall time delay value**,
>
> wherein the rise-time super generic value **represents rise times** and includes the rise time delay value stored in the rise time generic variable and the fall-time super generic value **represents fall times** and includes the fall time delay value stored in the fall time generic variable, **the rise-time super generic value being independent from the fall-time super**

generic value. (Emphasis added.)

Amended independent claim 18 recites, *inter alia*:

> a program memory for storing an SDF reducer, the program memory communicatively coupled to the VHDL standard delay file and the VHDL standard delay file analysis file, the VHDL standard delay file analysis file for selecting a rise time delay value and a fall time delay value in the VHDL standard delay file that **correspond to an instance of a logic gate in a logic model**, and for building a rise-time super generic value for the selected rise time delay value and a fall-time super generic value for the selected fall time delay value, the rise-time super generic value **representing rise times** and includes the rise time delay value stored in a rise time generic variable and the fall-time super generic value **representing fall times** and includes the fall time delay value stored in a fall time generic variable, the rise-time super generic value being independent from the fall-time super generic value. **(Emphasis added.)**

The present invention provides a more efficient method for the customization of gate delays that utilizes a VHDL package of array constants. The VHDL package of array constants replaces a significant amount of SDF file declarations for back annotation. The VHDL package of constants is efficient because it only has to be as large as the correlation of the delays, which can be quite significant when delay values are typically clustered around a range of values. Page 18, lines 9-10 of the instant specification. The back annotation process for the gate delays consists merely of resolving constant values for the fixed equations for the delay generics in the VHDL that describe gate behavior for the technology. These delay equations are formulated to depend **on just two generics** (a rise-time super generic and a fall-time super generic) per gate instance. Page 28, lines 7-9 of the instant specification.

However, the two generics of the present invention are defined in the claims such that "the rise-time super generic value [is] **independent** from the fall-time super generic value" and **there is no dependency between the rise and fall delay specifications**.

As noted by the Examiner on page 3 of the Office Action, Balaji utilizes tpd_* generics that hold delay value **pairs**.

The present invention breaks the prior-art practice of delay value pairing and opens up the realm of significant size savings due to breaking this dependency. This decoupling of the "rise/fall pair dependency" allows for many more matches in delay values, which is one of the keys to significant size reduction in the HDML file size. Also the super generics encompass more delays than the single delay generic of a single gate instance as in the cited prior art. A key capability of the present invention is that only two generics are needed to define all of the generic types for a gate instance (this is independent of the chip size, which scales well). Additionally, the rise-time super generic and the fall-time super generic allows for more than one prior-art generic to be depicted in a single super generic declaration.

Independent claims 1, 11, 18, and 25 have been amended to further clarify that the present invention breaks the rise/fall delay pair dependency of the prior art, as has been discussed above. The claims have been further amended to clarify that the present invention only supplies two super generics per gate instance and that the super generics can accommodate all traditional generic statements in one single generic for a gate instance in the SDF.

The Examiner cites 35 U.S.C. § 102(b) and a proper rejection requires that a single reference teach (i.e., identically describe) each and every element of the rejected claims as being anticipated by Balaji.[1] Because the elements in independent claims 1, 9, 11, 18, 25, and 33 of the instant application are not taught or disclosed by Balaji, the apparatus of Balaji does not anticipate the present invention. The dependent claims are believed to be patentable as well because they all are ultimately dependent on either of the independent claims 1, 9, 11, 18, 25, and 33. Accordingly, the present invention distinguishes over Balaji for at least this reason. The Applicants

---

[1] See MPEP §2131 (Emphasis Added) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim."

respectfully submit that the Examiner's rejection under 35 U.S.C. § 102(b) has been overcome. The Examiner should withdraw the rejection of these claims.

(28-30) Allowable Subject Matter

The Applicants wish to thank Examiner SHARON for indicating the allowable subject matter of claims 9 and 33. The Applicants have elected to amend claims 9, 10, 33, and 34, solely for the purpose of expediting the patent application process in a manner consistent with PTO's Patent Business Goals (PBG), 65 Fed. Reg. 54603 (September 8, 2000). Specifically, claims 9 and 33 have been rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 10 and 34 now depend from amended independent Claims 9 and 33, respectively. The Applicants submit that, in view of the amendment and remarks above, Claims 9, 10, 33, and 34, are now in condition for allowance, which allowance is respectfully requested.

CONCLUSION

The foregoing is submitted as full and complete response to the Official Action mailed August 4, 2005, and it is submitted that Claims 1-34 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of Claims 1-34 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

In this Response, Applicants have amended certain claims. In light of the Office Action, Applicants believe these amendments serve a useful clarification

purpose, and are desirable for clarification purposes, independent of patentability. Accordingly, Applicants respectfully submit that these claim amendments do not limit the range of any permissible equivalents.

Applicants acknowledge the continuing duty of candor and good faith to disclose information known to be material to the examination of this application. In accordance with 37 CFR § 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and the attorneys.

The present application, after entry of this amendment, comprises thirty-two (32) claims, including six (6) independent claims. Applicants have previously paid for thirty-four (34) claims including six (6) independent claims. Applicants, therefore, believe that a fee for claims amendment is currently not due.

If the Examiner believes that there are any informalities that can be corrected by Examiner's amendment, or that in any way it would help expedite the prosecution of the patent application, a telephone call to the undersigned at (561) 989-9811 is respectfully solicited.

The Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account **50-1556**.

In view of the preceding discussion, it is submitted that the claims are in condition for allowance. Reconsideration and re-examination is requested.

Respectfully submitted,

Date: November 4, 2005

By: _____
Scott Smiley, Reg. No. 55,627
Attorney for Applicants

By: _____
Jose Gutman, Reg. No. 35,171
Attorney for Applicants

FLEIT, KAIN, GIBBONS, GUTMAN BONGINI & BIANCO P.L.
551 N.W. 77th Street, Suite 111
Boca Raton, FL 33487
Tel (561) 989-9811
Fax (561) 989-9812